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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/462,994	01/14/2000	UDO SCHWALKE	P99.2666	5747

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/462,994	Applicant(s) SCHWALKE ET AL.	
	Examiner Brook Kebede	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-13,15-18,20 and 21* is/are rejected.

7)☒ Claim(s) *14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Germany on July 18, 1997. It is noted, however, that applicant has not filed a certified copy of the UNKNOWN application as required by 35 U.S.C. 119(b).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "said conductive filler structure being conductively connected to said doped region" must be shown or the feature(s) canceled from the claim(s). As shown in Figs. 3-7, the conductive filler structure (72) is placed on the insulation trenches (2) (i.e., STI shallow trench isolation) region. However, the doped region (3) located on the sides and underneath of STI region (2), so that the said conductive filler structure (72) can not be conductively connected to said doped region (3). No new matter should be entered. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim11 objected to because of the following informalities:

Claim 11 recites the limitation "said substrate" in line 3. As suggestion, change "said substrate" to --said semiconductor substrate-- in order to maintain consistency throughout the claim language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 11-13, 15-18, 20 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Uehara et al. (US/5,698,902).

Re claim 11, Uehara et al. disclose an integrated circuit arrangement having at least one doped region (21 21a 21b 11) is provided in a semiconductor substrate (10); a plane arranged on a surface of the semiconductor substrate (10) having a number of conductive useful structures (50a) (i.e. a gate electrode) and at least one conductive filler structure (50b) (i.e., a dummy gate or resistor); and the conductive filler structure (50b) is conductively connected to the doped region (21) (see Figs. 6-9(e)).

Re claim 12, as applied to claim 11 above, Uehara et al. disclose all the claimed limitation including the limitation a planarizing insulation layer (32) surrounding the conductive

useful structures (50a); and wherein the conductive useful structures (50a) and the conductive filler structure (50b) exhibit essentially the same height (see Fig. 6).

Re claim 13, as applied to claim 11 above, Uehara et al. disclose all the claimed limitation including the limitation a contact (31) connecting the conductive filler structure (50b) to the doped region (21 11) via a via hole (i.e. the contact used to form withdrawn electrode (31) (see Figs. 6-9(e)).

Re claim 15, as applied to one of the claims 11 above, Uehara et al. disclose all the claimed limitation including the limitation wherein the conductive useful structures (50a) are gate electrodes; and wherein the conductive filler structure (50b) contains the material of the gate electrode (see Figs. 6-9(e)).

Re claim 16, as applied to one of the claims 11 above, Uehara et al. disclose all the claimed limitation including the limitation whereby the doped region (21 11) is a doped well or the semiconductor substrate (10) (see Figs. 6-9(e)).

Re claim 17, as applied to on of the claims 1-6 above, Uehara et al. disclose all the claimed limitation including the limitation a metallization layer (34) is arranged above the plane wherein the conductive filler structure (50b) is arranged; and a further contact connecting the conductive filler structure (50b) and the metallization layer (34) (i.e. the contact a buried layer is formed) (see Figs. 6-9(e))

Re claim 18, Uehara et al. disclose a method for manufacturing an integrated circuit arrangement comprising: forming a doped region (21 1) in a semiconductor substrate (10); forming a plane (16x) on a surface of the semiconductor substrate (10) by applying a nd structuring a conductive useful structures (50a) and at least one conductive filler structure (50b) producing an insulation layer (32) surrounding and covering the conductive useful structures

(50a) and the conductive filler structure (50b); and producing a conductive connection between the conductive filler structure (50b) and the doped region (21 11) (see Fig. 6-9(e)).

Re claim 20, as applied to claim 18 above, Uehara et al. disclose all the claimed limitations including producing a metallization layer (34) above the plane wherein the conductive filler structure (50b) is formed; producing a further contact (33) connecting the conductive filler structure (50b) connecting to the metallization layer (34) (see Fig. 6-9(e)).

Re claim 21, as applied to one of the claims 11 above, Uehara et al. disclose all the claimed limitation including the limitation whereby the doped region (21 11) is the semiconductor substrate (10) (see Fig. 6).

Allowable Subject Matter

7. Claims14 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Liaw et al. (US/5,866,449), Pan et al. (US/5,869,396), Harvey et al. (US/6,207,543), and Pan (US/6,300,653) also disclose similar inventive subject matter.

Correspondence

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
October 23, 2002